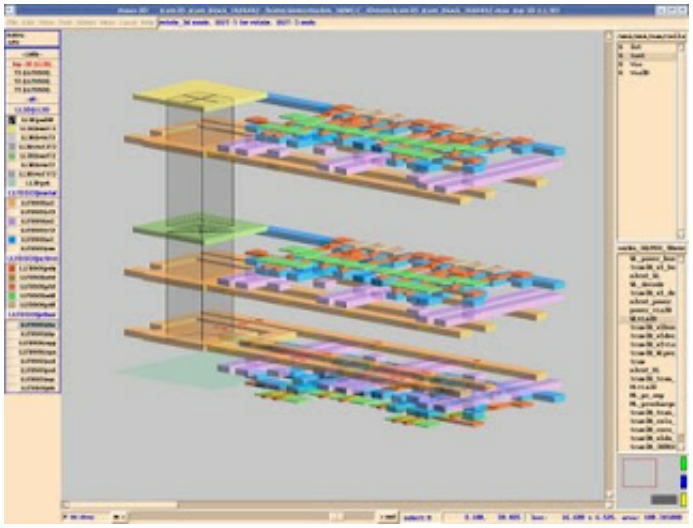
3D EDA Tools – Coming out of the Woodwork

That didn't take long. A post about one EDA tool introduction inspired a comment about a 3D layout editor that's been on the market for 2 years. A mention of said comment in Tuesday's email update and an email to the individual who posted the comment brought immediate response. This is the beauty of blogging; it results in an almost instantaneous sharing of information and inspires collaboration.



According to Mark Mangum, sales manager for EDA tools and chip design tools at Micro Magic, Inc, the company's layout editor, MAX 3D, handles the physical design of the chip, and is particularly suited to TSV design. He explained that its ability to manage separate wafer levels with individual tech files is more effective than relying on a "super tech file" to handle the whole design. With this approach, each wafer level maintains its own tech file throughout the design process.There is an additional tech file for the interconnect. In addition, the tool's speed and capacity is ideal for handling the size and complexity of TSV designs. A slower editor tends to decrease performance drastically.

Three important elements of good EDA tools are programmability, customizability, and compatibility with other tools in the toolbox. Mangum assured me that MAX 3D was developed with these considerations in mind. "Integration is a key selling point for our customers, so we've made an effort to make our tools work with others." he said, adding that the tool was developed for "open architecture", with ASCII data files and open source scripting language. OpenAccess support was added for design data files due to customer demand, and is continually updated. To handle Pcell design data, a Pcell interpreter from IPL was added to allows users to read their Pcell data. "MAX-3D has real time design rule checking (DRC), but because many customers use Mentor Calibre for signoff DRC, a direct interface to Calibre was added. We also support industry standard file formats such as GDSII, LEF, DEF, etc. so MAX-3D users won't have to worry about "vendor lock-in" of file formats - for design data, cells, or generators," he said.

Mangum told me MAX-3D is being used by several universities, including MIT, Lincoln, Cornell, North Carolina State, Penn State. Six companies have also incorporated it into their processes, mainly for developing test chips.

Are there other 3D tools in the works at Micro Magic? Mangum says yes, but is hush-hush about

it. "We are working on some packaging-related development with a customer, but no word on when we'll be discussing it," he said. Simulation and verification are big blind spots in the industry right now, he added, but rumor has it, Mentor has something in the works on this.

I know one of Micro Magic's customers is happy with the performance of the company's tools. An unsolicited endorsement appeared in my inbox shortly after I mentioned the product in my email. Gretchen Patti, technical communications specialist for Tezzaron Semiconductor, stated simply, yet enthusiastically. "About Micro Magic: Their tools are real! We use them." That's pretty much all I needed to know. – F.v.T.

Francoise von Trapp
02/26/2009 - 6:58am
# of views: *2048*

Source URL: http://www.infoneedle.com/posting/21768